WHAT IS CLAIMED IS:

1. A method for arranging a plurality of memory cells in a predetermined direction along which at least one pair of bit lines extend and to which the memory cells are connected, the method comprising:

arranging a first memory and a second memory alternately and adjacent to each other in a predetermined direction, wherein the second memory cells have a symmetric geometrical relationship with the first memory cell with respect to an axis perpendicular to the pair of bit lines;

arranging a non-cell region adjacent to one of the first and second memory cells in the predetermined direction; and

arranging a third memory cell having an asymmetric geometrical relationship with the one of the first and second memory cells with respect to the axis in the predetermined direction adjacent to the non-cell region.

2. The method according to claim 1, wherein:

said arranging a first memory and a second memory alternately includes arranging the first memory cell and the second memory cell so that the first memory cell and the second memory cell are symmetric to each other relative to the axis; and

said arranging a third memory cell includes arranging the third memory cell so that the third memory cell is asymmetric to the one of the first and second memory cells.

3. The method according to claim 1, wherein said arranging a third memory cell includes arranging the third memory cell and the one of the first and second memory cells oriented to be in the same direction.

4. The method according to claim 1, wherein said arranging a third memory cell includes arranging the third memory cell to have a geometrical relationship with the one of the first and second memory cells so that parallel movement of the third memory cell in the predetermined direction overlaps the third memory cell with the one of the first and second memory cells.

5. The method according to claim 1, wherein the non-cell region is provided for each predetermined number of memory cells, the predetermined number of memory cells each including a transistor, the method further comprising:

arranging a contact connected to a backgate of the transistor in the non-cell region.

6. The method according to claim 5, further comprising:

arranging the first and second memory cells so that the first and second memory cells share a bit line contact connected to a source and a drain of the transistor.

7. The method according to claim 1, wherein the plurality of memory cells are SRAM memory cells.

8. A method for arranging a plurality of memory cells along at least one pair of bit lines extending in a predetermined direction, wherein the memory cells each have a first side and a second side that are parallel to a perpendicular axis, which is perpendicular to the at least one pair of bit lines, the method comprising:

forming a first sub array with at least one first memory cell unit including an even number of memory cells

arranged adjacent to one other in the predetermined direction so that the adjacent memory cells have a symmetric geometrical relationship relative to the perpendicular axis, wherein the first side is defined on each of opposite ends of the first memory cell unit in the predetermined direction;

forming a second sub array with at least one second memory cell unit including an even number of memory cells arranged adjacent to one another in the predetermined direction so that the adjacent memory cells have a symmetric geometrical relationship relative to the perpendicular axis, wherein the second side is defined on each of opposite ends of the second memory cell unit in the predetermined direction;

alternately arranging the first sub array and the second sub array in the predetermined direction with a non-cell region located in between.

9. The method according to claim 8, wherein the at least one pair of bit lines includes a first bit line and a second bit line, which is complementary to the first bit line, wherein the first memory cell unit is one of a plurality of first memory cell units, and the second memory unit is one of a plurality of second memory cell units, the method further comprising:

arranging two of the first memory cell units adjacent to each other in the predetermined direction to share at least the second bit line; and

arranging two of the second memory cell units adjacent to each other in the predetermined direction to share at least the first bit line.

10. The method according to claim 9, further

comprising:

providing a plurality of bit line contacts in each bit line so that two memory cells adjacent to each other in the predetermined direction share the bit line contacts, wherein the bit line contacts in the first bit line and the bit line contacts in the second bit line are arranged alternately in the predetermined direction.

11. The method according to claim 8, wherein said alternately arranging the first sub array and the second sub array includes using the same number of the first sub array and the second sub array.

12. The method according to claim 8, wherein said alternately arranging the first sub array and the second sub array includes using a different number of the first sub array and the second sub array.

13. The method according to claim 8, wherein the number of memory cells configuring the first memory cell unit is the same as the number of memory cells configuring the second memory cell unit.

14. The method according to claim 8, wherein the non-cell region is one of a plurality of non-cell regions, each provided for a predetermined number of memory cells arranged in the predetermined direction, and the predetermined number of memory cells each include a transistor, the method further comprising:

arranging a contact connected to the backgate of the transistor in each of the non-cell regions.

15. The method according to claim 8, further

comprising:

arranging a source and a drain of a transistor connected to a bit line contact of the bit lines so that adjacent memory cells share the contact in each sub array.

16. The method according to claim 8, wherein the plurality of memory cells are SRAM memory cells.

17. A semiconductor memory device comprising:

a bit line extending in a predetermined direction; and

a memory cell array including a plurality of memory cells arranged along the bit line, the plurality of memory cells including:

a first memory cell;

a second memory cell adjacent to the first memory cell in the predetermined direction and having a geometric shape that is symmetric to the first memory cell with respect to an axis perpendicular to the bit line;

a non-cell region adjacent to the second memory cell in the predetermined direction; and

a third memory cell arranged adjacent to the non-cell region in the predetermined direction, wherein the third memory cell and the second memory cell have the same geometric shape and are oriented in the same direction.

18. The semiconductor memory device according to claim 17, wherein:

the first memory cell and the second memory cell are symmetric to each other with respect to the axis; and

the second memory cell and the third memory cell have an asymmetric geometric shape with respect to the axis.

19. The semiconductor memory device according to claim 17, wherein the third memory cell has a geometric shape so that parallel movement of the third memory cell in the predetermined direction overlaps the third memory cell with the second memory cell.

20. The semiconductor memory device according to claim 17, wherein the first memory cell and the second memory cell are in a mirror image relationship with respect to a plane perpendicular to the predetermined direction.

21. A method for designing a memory cell array having a pair of bit lines extending in a predetermined direction, the method comprising:

arranging a first memory cell and a second memory cell so that the first and second memory cells have a mirror image relationship with respect to a plane perpendicular to the pair of bit lines;

arranging a non-cell region adjacent to the second memory cell in the predetermined direction; and

arranging a third memory adjacent to the non-cell region in the predetermined direction so that the third memory cell is oriented in the same direction as the second memory cell.

22. A semiconductor device comprising:

a first bit line pair extending in a predetermined direction;

a second bit line pair extending in the predetermined direction;

a first memory cell connected to the first bit line pair and the second bit line pair;

a second memory cell connected to the first bit line pair and the second bit line pair adjacent to the first memory cell, wherein the first memory cell and the second memory cell are in a mirror image relationship with respect to a plane perpendicular to the bit line;

a non-memory cell adjacent to the second memory cell; and

a third memory cell adjacent to the non-cell region, wherein the third memory cell and the second memory cell are oriented in the same direction.

23. A semiconductor memory device including a bit line extending in a predetermined direction, the semiconductor memory device comprising:

a first memory cell;

a second memory cell adjacent to the first memory cell in the predetermined direction and being symmetric to the first memory cell with respect to a plane perpendicular to the predetermined direction;

a non-cell region adjacent to the second memory cell;

a third memory cell adjacent to the non-cell region and having an asymmetric geometrical relationship with the second memory cell with respect to the plane; and

a fourth memory cell adjacent to the third memory cell in the predetermined direction and symmetric to the third memory cell with respect to a plane perpendicular to the predetermined direction.

24. The semiconductor memory device according to claim 23, wherein the third memory cell and the second memory cell are oriented in the same direction.